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Effects of Scaling of Junctionless Transistor Parameters with Silicon Dioxide (Sio_2) and Silicon Nitrate (Si_3N_4) Gate Oxides on the Electrical Characteristics of the Devices

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ABSTRACT: This research investigated the effects of scaling of parameters of junctionless transistors (JLT) with SiO_2 gate oxide and Si_3N_4 gate oxide on the electrical characteristics of the two devices. It also compared the electrical performance of the two devices as a way of replacing the conventional SiO_2 gate oxide with high-k dielectric such as Si_3N_4 gate oxide. Different JLT were designed and simulated using a technology computer aided device software, sentaurus and extracted the electrical characteristics such as Threshold voltage, subthreshold slope, drain induced barrier lowering, on-state current etc. It was observed that leakage current, DIBL, SS as well as on-state current were significantly improved using Si_3N_4 as gate oxide in JLT. As a result, on-state to off-state current ratio was greatly increased, hence the speed of the device. The performance was significantly increased to approximately 10^9 using Si_3N_4 material for gate length of 10nm and nanowire diameter of 10nm. All these were achieved because of the high dielectric constant, k of the Si_3N_4 which is higher than that of SiO_2. Similarly, Si_3N_4 has also has high energy band gap which considerably help in reducing the leakage current and other short channel effects (SCEs).

KEYWORDS: Silicon Nitrate, Gate oxide, Leakage current, Junctionless transistor, Silicon dioxide,Dielectric constant

1. INTRODUCTION

The scaling process allowed more transistors to be packed in a smaller chip area and hence enhance the functionality of SCEs. MOSFET typically used in industries due to its small size, and can be fabricated in a single integrated circuit with millions numbers [1]. However, the scaling of conventional planar transistor has reached its limit which lead to increase in short channel effects (SCEs) and sensitivity to process variation. SCEs comprises of Drain Induced Barrier Lowering (DIBL), subthreshold slope (SS), limitation imposed on electron drift characteristics in the channel, increase in threshold voltage variation, reduction in I_{ON}/I_{OFF} ratio and increase of leakage current causing the scaling of conventional CMOS transistors in sub 10nm technologies almost impossible [2].

In MOSFET, the Leakage currents drastically increased due to tunneling of electrons when the gate thickness oxide (t_{ox}) is below 2nm [3]. It can lead to low reliability and high power consumption of the device. High k dielectrics such as Si_3N_4 is a good alternative to replace the conventional SiO_2 thereby increasing the gate capacitance without affecting the leakage [4].

This research is expected to investigate and analyze the effects of scaling of junctionless field effect transistor (JFET) parameters such as gate length, nanowire diameter and different gate oxides on the performance of the JLT. Silicon dioxide (SiO_2) and silicon nitrate (Si_3N_4) gate oxides will be use in this study.

2. PREVIOUS WORK

Due to larger tunneling path and the energy gap between the conduction band and fermi level of the JLT with Si_3N_4 gate oxide in the subthreshold state compared to SiO_2 device in the drain region [5]. High k increases the capacitance of the device with SI_3N_4 thereby increasing the charge holding capacity due to large capacitance of the device [6]. Si_3N_4 materials have good chemical and thermal stability on silicon material [7]. When the gate oxide thickness is reduced to 1nm, high leakage current was observed in JLT with SiO_2 gate oxide. higher dielectric constant in high-k materials help to reduce the leakage current in the device [8].

Surface contact area between the channel and the oxide layers and the thermal conductivity of the oxide materials are the main factors that define the temperature at the center of the channel. Transistor having SiO_2 as the back oxide layer and Thermal conductivity of the oxide materials and the surface contact area between the channel and the oxide layers are the main factors that define the temperature at the center of the channel. Higher electric resistance of Si_3N_4 thin films and its smaller crystallite size caused very low leakage current than SiO_2 gate oxide. Si_3N_4 exhibits better Of-state current and gives suitable switching of the device. Therefore, improving the device I_{ON}/I_{OFF} ratio [9].

Gate control was improved in double hetero gate oxide device with Si_3N_4 on the top oxide. Due to the compatibility of lattice constant of SiO_2 and silicon, low-k dielectric can be used over

silicon body. The leakage current was significantly decreased when the permittivity coefficient as well as the oxide thickness of the transistor decreased [10]. Because of the absent of strict requirement of high concentration gradient makes the scaling of gate oxide layers possible for t_{ox} of 1nm. High leakage current was observed in the device with SiO_2 gate oxide for gate thickness oxide of 1nm. Using High metal gate work function and induced gate stack used for neutral biomolecule species detection to improve the performance of the transistor. The result shows substantial improvement for SCEs when they were all examined for the study of the biosensor response [11].

3. RESEARCH METHODOLOGY

This research was designed to investigate the effects of scaling of parameters of junctionless transistors (JLT) with SiO_2 gate oxide and Si_3N_4 gate oxide on the electrical characteristics of the two devices. It also compared the electrical performance of the two devices as a way of replacing the conventional SiO_2 gate oxide with high-k dielectric such as Si_3N_4 gate oxide.

Transistors of different gate lengths (L_G) and nanowire diameter (d_{NW}) will be designed, simulate, compared and analyzed to obtain the most optimal devices. SDE and sdevice tools of sentaurus TCAD will be use to simulate and extract the electrical properties of the devices. Lombardi mobility model and Philips unified mobility model will be applied electric field and doping dependent mobility degradation. A thin-film heavily doped silicon nanowire with a gate electrode that controls the flow of current between the source and drain will be use. The electrical characteristics will be appraised and compared with the inversion mode device for different gate length and nanowire diameter. Electrical characteristics such are drain induced barrier lowering (DIBL) and subthreshold slope (SS) will be extracted and may leads to low leakage current as well as a high On-state to Off-state current ratio. The performance of the transistors will be expected to improve by changing silicon dioxide (SiO_2) with silicon nitrate (Si_3N_4).

Philips unified mobility model and Lombardi mobility model were considered as field- and doping-dependent mobility degradation. For Dominant generation and recombination process in silicon and other indirect energy band gap materials, Shockley–Read–Hall was used. Also, the SRH dominate in direct band gap materials under conditions of very low carrier densities or very low level injection. Auger recombination model and Fermi–Dirac statistics were also used as design model. Electrical parameters of nanowire junctionless transistor with HfO_2 gate oxide was compared with that of Si_3N_4 gate oxide device to determine the best optimized device.

4. RESULT AND DISCUSSION

In this research, the parameters used for both junctionless transistors, JLT (with SiO_2 and Si_3N_4 gate oxides) are the same. The gate lengths, L_G of the devices varied from 10 to 50 nm. The gate thickness oxide, t_{ox} is 1nm and the Silicon nanowire diameter was 10 nm. SiO_2 and high-k dielectric materials, Si_3N_4 devices of different L_G and d_{NW} were also designed and simulated to obtained electrical characteristics using Sentaurus TCAD. High-k dielectric was used in the JLT device structure to improve the electrical characteristics and reduce the SCEs. The electrical characteristics and performance of the devices was analyzed which are V_{TH}, ON-state current, OFF-state current, DIBL, SS and the ON-state-to-OFF-state current ratio.

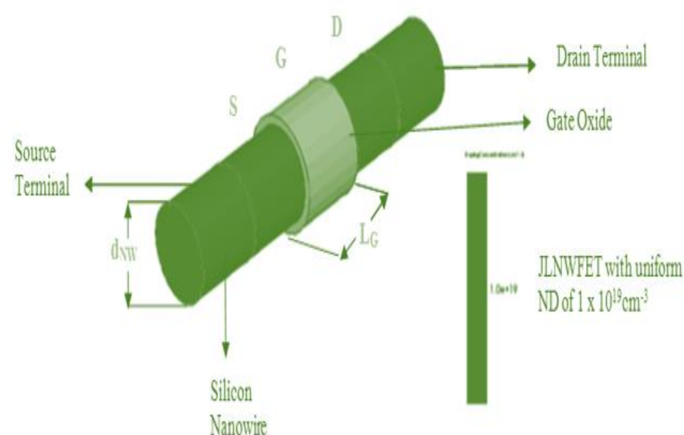

Fig. 1: Junctionless Field Effect Transistor

Using a constant diameter of nanowire of 10nm, gate and drain voltages, V_G and V_D of 1V, the result shown that device with Silicon Nitrate (Si_3N_4) gate oxide exhibits better subthreshold slope than device with Silicon Dioxide (SiO_2) as shown in figure 2. This is due to the higher dielectric constant and excellent thermal stability of Si_3N_4. It was observed that for gate length (L_G) 10nm, the subthreshold slope (SS) of device with Si_3N_4 is 68.5mV/dec which close to the theoretical limit of SS is 60 mV/decade, while device with SiO_2 has 74.9mV/dec for the same L_G of 10nm. SS improves further as the L_G increases to 40nm. SS became lower than the theoretical limit, 60 mV/dec when L_G is 50nm in both the two transistors.

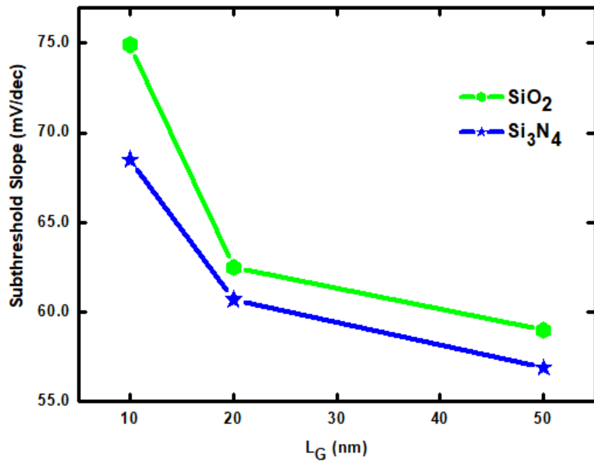

Fig. 2: SS of the two Junctionless Transistor devices with constant dNW of 10nm

Threshold voltage (V_{th}) is the gate voltage required to cause the inversion in a MOSFET. It is a function of oxide layer thickness which increases when the oxide thickness (t_{ox}) of a JLT increases. In figure 3, it was observed that JLT with Si_3N_4 gate oxide exhibits higher V_{th} than JLT with SiO_2 gate oxide. For 20nm gate length, the JLT with Si_3N_4 gate oxide has V_{th} of 0.46V compared to JLT with SiO_2 gate oxide which has 0.41V. The figure also reveals that V_{th} increases when the L_G increased.

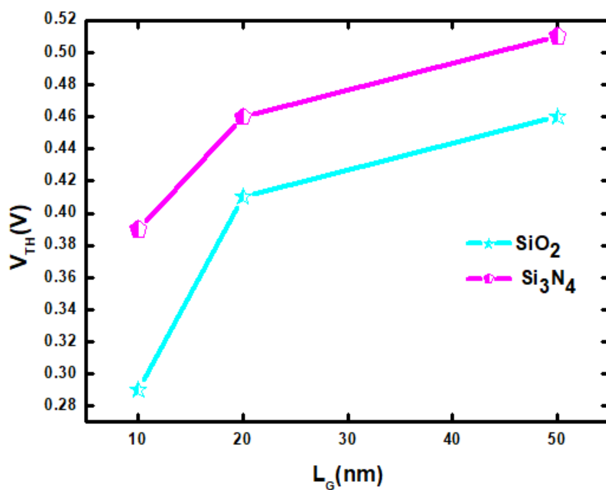

Fig. 3: Threshold Voltage of the two JLT devices

Drain induced barrier lowering (DIBL) is expected to have a very low due to the absent of junction in the junctionless FET. It can be observed in figure 4 that the JLT with Si_3N_4 gate oxide demonstrates lower DIBL than JLT with SiO_2 gate oxide because the high-k dielectrics can help to minimize this DIBL effect very effectively when the gate length is small. Similarly, for 10nm gate length, DIBL was significantly improved in the device with Si_3N_4 gate oxide having 47.0mV/V compared to 79.7mV/V of the device with SiO_2 gate oxide. It was also learned that DIBL decreases as the gate length increased.

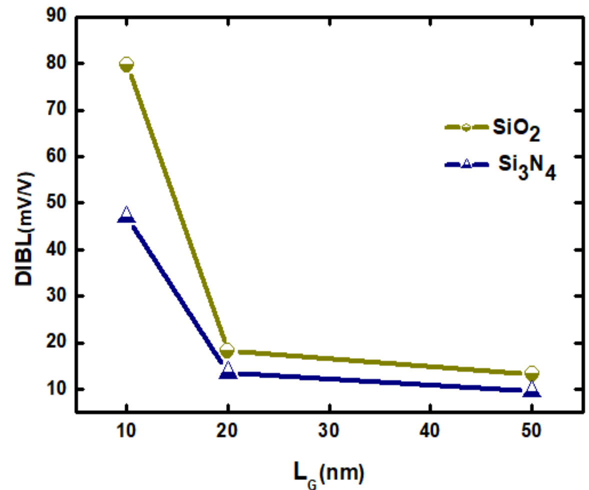

Fig. 4: Comparison of DIBL of the Si_3N_4 and SiO_2 gate oxide devices

Figure 5 shows that Si_3N_4 exhibits higher on-State current (I_{ON}) due small cross-sectional are of the nanowire and high doping concentration which results to high electron mobility in the channel junction because of high movement of electrons from source to drain, hence higher current flows. JLT device with Si_3N_4 gate oxide has I_{ON} of 8.3 x 10^{-6}A for gate length of 50nm, while device with SiO_2 gate oxide has I_{ON} of 7.8 x 10^{-6}A having the same L_G. Similarly, the plots show that the on-state current decreases as the L_G increase further.

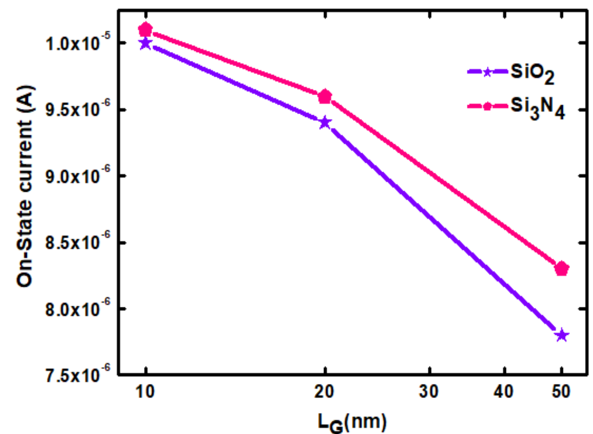

Fig. 5: On-state current of the Si_3N_4 and SiO_2 gate oxide Junctionless FET

Due to small nanowire diameter (d_{NW}) or small cross-sectional area of the nanowire and metal gate work function, the Off-state current (I_{OFF}) or leakage current of the two devices decreases because of the full depletion of the heavily doped channel.

Consequently, it was found that Si_3N_4 gate oxide device demonstrates I_{OFF} than SiO_2 gate oxide device. For 10nm gate length, Si_3N_4 device, the Off-state current was significantly

improved having 2.3 x 10^{-13}A compared to SiO_2 device which has 2.7 x 10^{-11}A. However, as the gate length increases the Off-state improved further.

Because of the higher On-state current and lower Off- state current, the On-state to Off-state current ratio increased. This could lead to the increase of the performance of microprocessor of the computer. However, there are other factors that must also be consider to improve the overall performance of the microprocessor.

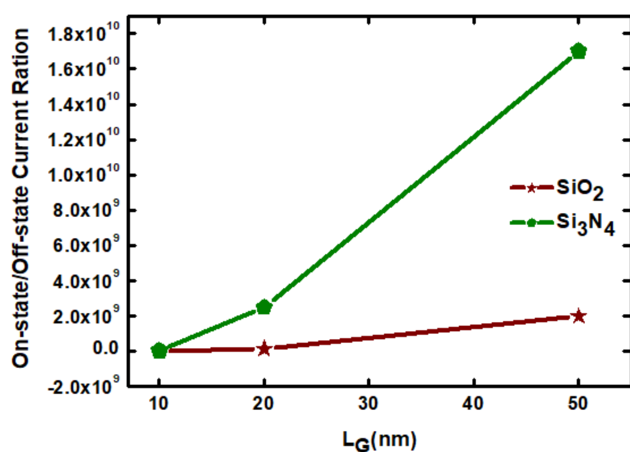

Fig. 6: On-state to Off-state current ratio of the two JLT devices

In figure 6, the On-state to Off-state current ratio of the Si_3N_4 device was significantly improved better than SiO_2 device as shown. For L_G of 20nm, the On-state to Off-state current ratio of the Si_3N_4 device was found to be 2.5 x 10^9 compared to that of SiO_2 device which has 1.5 x 10^8. Similarly, the ratio increases further when the gate length increases.

5. CONCLUSION

This work discovered that junctionless transistor with Si_3N_4 gate oxide device exhibits momentous electrical characteristics than the JLT with SiO_2 for L_G lower than 20 nm. Furthermore, SCEs such as DIBL and subthreshold slope are extensively enhanced. Because of the small cross-sectional area and high doping concentration in the design, the on-state and off-state currents were significantly improved results to high on-state to off-state current ratio. The leakage and I_{ON} current in Si_3N_4 device were significantly improved due to the high dielectric constant and high gate capacitance. Consequently, faster switching speed of the Si_3N_4 device was observed more than SiO_2 device as a result of highly improved On-state to Off-state current ration in the device.

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