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Design and Analysis of Two-Stage Operational Transconductance Amplifier with Compensation Capacitor

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ABSTRACT

For designing of high-performance analog circuits is still a hard task towards reduced supply and increased unity bandwidth. OTA is the basic element with highest power dissipation in many applications. In a handheld device, low power consumption is very essential so it is a challenge to design a low-power OTA with higher gain, low power dissipation and high CMRR. There is a compromise between again, speed, power and unity gain bandwidth because all these parameters depend on each other. A novel design procedure for CMOS two-stage operational transconductance amplifier is presented in this paper. A compensation compensation method for operational transconductance amplifiers is proposed, which poses no power overhead compared to Miller compensation, while improving the 3-dB bandwidth, the unity gain frequency, and the Power dissipation. In this design supply voltage is 1.8v and simulated by using CADENCE VIRTUOSO tool at 180nm technology. The open loop gain of this OTA is about 70 dB, GBW is 500 MHz, CMRR is 117 dB and Power Dissipation is 174.25.

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KEYWORDS: ***Operational trans conductance amplifier (OTA); GBW; CMRR; DC Gain; Power Dissipation.***

1.INTRODUCTION

Linearly CMOS techniques have gathered significant progress over the last few years to offer low-power high performance mixed analog building blocks like operational amplifiers (op amp), buffers, comparators, etc.If CMOS technology used in any analog circuit, the total trans conductance would be constant if the transistors at the input are biased in weak inversion [1]. However, if they are biased in strong inversion, transconductance will be increased by 40%.Operational Trans conductance amplifier (OTA) can be considered as an exclusive case of Op-Amp in Voltage controlled current source form. Its differential input voltages provide an output current but along with it, it has an additional input current to control trans conductance of amplifier. Operational trans conductance amplifiers (OTA) shown in the Fig.1 are basic building elementsfor the design of analog high-performance systems [2]. The voltage at input is V_{in+} and V_{in-} and the current at the output is I_O, these are related with each other by proportionality constant trans conductance (g_m). I_{bias} is the biasing current of the diode at the anode terminal.Where, V_{IN} is the differential input voltage. Its structure is very robust and simple, due to which provides novel values for its electrical parameters such as dc gain, gain bandwidth and CMRR, etc

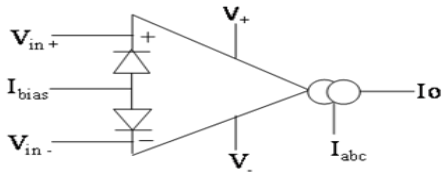

Fig.1 Basic block diagram of OTA

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$$I_0 = g_m V_{IN} \quad (1)$$

$$I_O = g_m(V_{IN+} - V_{IN-}) \quad (2)$$

$$\text{Output voltage}(V_O) = I_O . R_{LOAD} \quad (3)$$

These OTA are used in a wide variety of applications, such asRC continuous-time filters, sigma-delta ADC design, data converters, modulators, mixers,instrumentation amplifier and four-quadrant multiplier[3][4][5][6].It is very crucial to design an amplifier with both high bandwidthand high gain. For high gain amplifier we use multi-stage designs, or cascade structures with long channel length transistors biased at low current levels. For high bandwidth amplifiers use single-stage designs with short channel length transistors biased at high current levels [4]. The design procedure is based on the following main parameters: DC gain,unity gain-bandwidth (UGB), input common mode range (CMR), load capacitance (C_L), power dissipation, Phase margin, and common mode rejection ratio (CMRR) [7].The proposed OTA in this paper describes in detail on ways to enhance CMRR for the application data acquisition system using common mode feedback circuit (CMFB).Common-mode voltages of the differential-mode circuit are stabilizing by using Common-mode feedback circuits and due to which thestability problems are not an issue for designing CMFB's for voltage-mode systems [8].Data Acquisition system is the process in which the signal is sampled and that measure real word physical values and modify the resulting samples into digital value that can be employed by computers. The constituents of data acquisition systems includeSensors, signal conditioning circuitry and Analog-to-digital converter [9]. This paper is organized as follows.Two-stage OTA is described in section 2, Telescopic OTA circuit design is described in section 3. Section 4 presents the Telescopic OTA with CMFB circuit. Section 5 presents the CMFB circuit. Section 6gives simulation results. Finally some concluding remarks are provided.

2. THE DESIGN OF TWO STAGE OTA

The two stage OTA is shown in the fig.2 the first stage is a differential input with current mirror load and the gain of the op-amp is mainly depends on differential input stage with single-ended output, the DC gain does not depends on the choice of N-channel or P-channel input pair. Generally N-channel transistors have more 1/f noise as compared to the P-channel transistors because of their majority carrier (holes) have less potential to be trapped in surface state [10]. The second stage is cascade of common gate with common source, due to which the stability of the output is effectively isolated from the input both electrically and physically, and the gain, bandwidth, slew rate, stability and input-output impedance is high. In cascaded design, the gain is boosted with more than one amplifying stage, the power consumption is increases and the frequency compensation requirement is also increases. There are some methods to improve the OTA gain e.g. positive feedback and a use of replica amplifier. Among all these methods a large number of powersare used to enhance the gain [2].

In this design we use miller compensation to compensate the pole which exists at the right half-pole. Compensation path is used for pole-zero compensation which increases the non-dominant pole frequency [14]. The compensation technique is based on eliminating the feed forward path from the first stage output to the OTA output. The current $Cc\frac{dvd}{dx}$ is flow in first stage output; the feed forward path is eliminated while still a dominant pole is produced due to the miller effect.

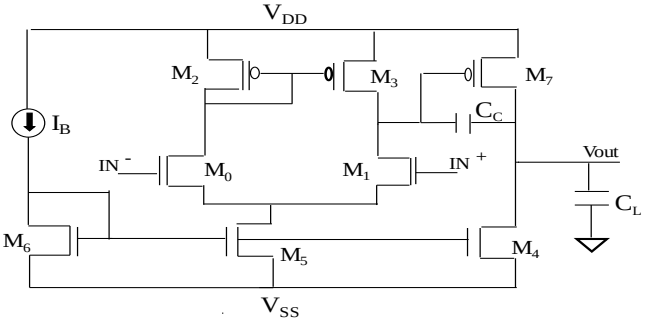

Fig 2 Schematic of two-stage OTA.

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The miller capacitance is $(1+A_2)\ C_C = A_2\ C_C$, where A_2 is thevoltage gain of second stage and v_d is the differential voltage [15]. The compensation capacitor is break into two capacitance C_M and C_{MO}. The technique described here provides stable operation for a much larger range of capacitive loads, as well as much improved power supply rejection over very wide bandwidths for the same basic op amp circuit.

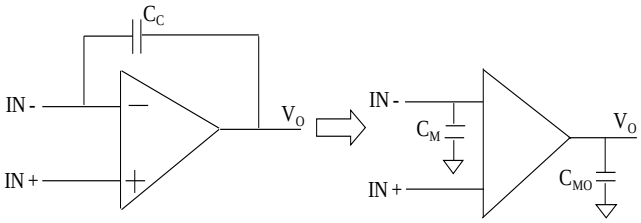

Fig 3. Compensation method

$$CM = Cc\ (1 + Av) \text{ and } Cmo = Cc(1+ 1\ Av\ ) \quad (4)$$

The DC gain is increased by adding compensation capacitor. The DC gain is 62dB by adding the compensation capacitor.

Table 1. Device sizes of proposed OTA

Transistors	Width(um)	Length(um)
NM1	1.08	0.18
NM2	13.5	1
NM3	2.16	1
NM4	1.08	0.18
NM5	2.16	1
PM0	2.5	0.18
PM1	31.14	0.18
PM2	2.5	0.18

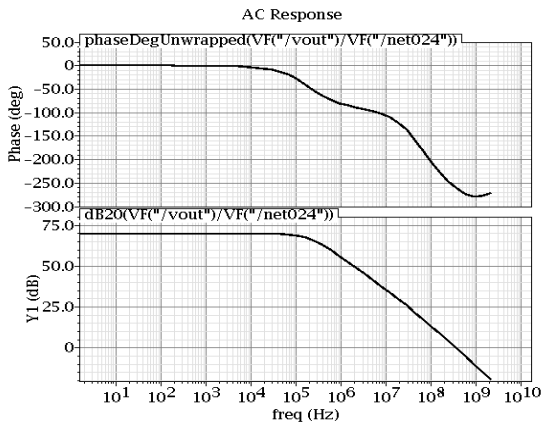

Fig 4. Simulated frequency response results

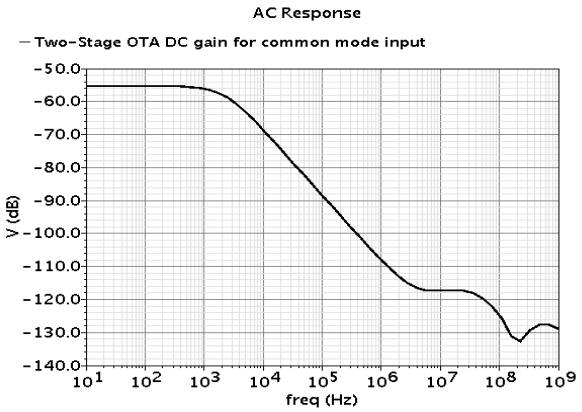

Fig 5.CMRR of the two-stage OTA.

CMRR = DC gain – CM gain (8)

` = 62-(-55) =117dB.

Table2. Performance comparison of the conventional and designed Two-stage OTA

Parameters	Conventional OTA [10]	Proposed OTA
Gain (dB)	61.41	70
UGB (MHz)	NA	500
PM (degree)	100.21	105
CMRR (dB)	not given	117
Supply voltage	0.7	1.8
Power Dissipation(µW)	235.25	174.75
Technology	0.045µm CMOS	0.18 µm CMOS

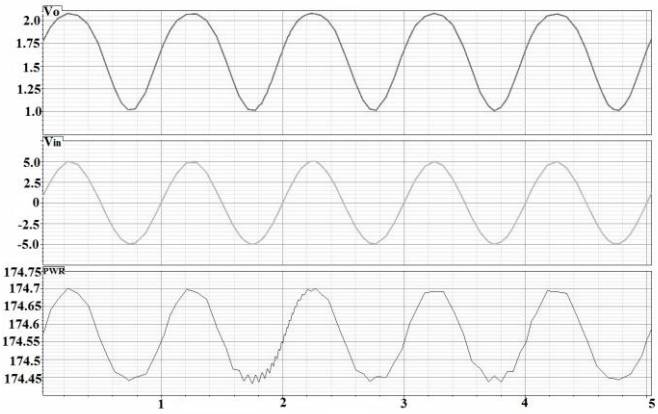

Fig 6. Transient Simulation of Two-Stage OTA

3. SIMULATION RESULT

The proposed OTA is designed in standard 0.18 □m CMOS technology. The performance of the proposed circuit is predicted by simulations running

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on CADENCE Virtuoso Tool. The device sizes of the circuit are given in Table 1. Performance analysis is shown in Table 2. Fig. 4 shows the frequency response of the proposed OTAwith a power supply of 1.8 V and a bias current of 50 nA.Simulations show that the DC gain is 70 dB, the unity gain bandwidth is 500MHz and the phase margin is 105°.The CM range output is shown in Fig. 5. The Transient Response is shown in Fig 6.

4. CONCLUSION

A 1.8-V Two-stage OTA is designed in this work. The circuit makes use of the Compensation capacitor to improve the DC gain. A concise bias circuit guarantees the OTA robust against the variations of fabrication and working conditions. Simulations show that DC gain is 70 dBin typical condition and keeps above 65 dB in all working conditions. This OTA is suitable for low-voltage, low-power applications, such as smart sensors.

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