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Study the Performance of Silicon-On-Insulator Based Junction Less Transistor Using MOS and FGMOS 6t-Sram Cells

Bubakari Joda[1], Mohammed A. Sule[2], Bashir I. Njodi[3], Abbas Adamu[4], Denis D. Jonathan[5]

[1]Department of Electrical/Electronic Engineering Technology, Federal Polytechnic Kaltungo, Nigeria.

[2,3,5]Department of Computer Engineering Technology, Federal Polytechnic Kaltungo, Nigeria.

[4]Department of Electrical/Electronic Engineering Tech. Federal Polytechnic N'yakShendam, Nigeria

ABSTRACT: In this research, a 6T SRAM cell comprises of two cross-coupled inverters and two access transistors was design and simulated using Sentaurus TCAD and Spice Simulator. The cross-coupled inverters are the memory part used to store the data. When the access transistors are turn ON, enabling the read/write operation. 6T SRAM using metal oxide semiconductor (MOS) and floating gate metal oxide semiconductor (FGMOS) of different node technologies at constant drain voltage (V_{dd}) of 0.35V were designed and simulated. Power dissipation and delay were computed for different technology nodes using MOS and FGMOS devices. It has been observed that 45nm technology node 6T SRAM cell demonstrated most optimized power dissipation as compared to 180nm, 90nm, and 65nm technology 6T-SRAM cells when we use MOS and FGMOS. In case of delay measurement, it was observed that device with FGMOS have most improved. This reduces the power dissipation, making the SRAM cell applicable for low power applications, and the use of FGMOS further decreases the power dissipation and delay of the 6T-SRAM cell.

KEYWORDS: static RAM, delay, power dissipation, junctionless, transistor.

1.0. INTRODUCTION

Conventional transistors need junctions to conduct current. PN junction is the common junction that could block and allow the flow of current in the channel. However, junctionless transistor (JLT) was introduced in order to solve the above challenges. JLT is a transistor that has no junction [1]. Figure 1 shows the device structure of junctionless transistor.

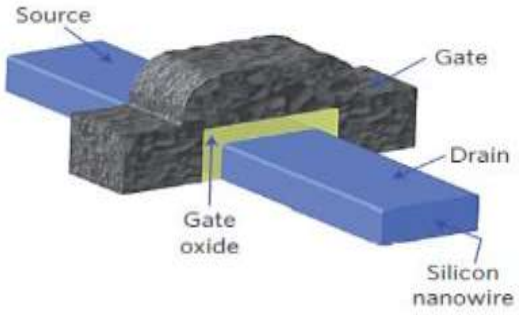

Fig. 1: Structure of a Junctionless Transistor

The junctionless transistor contain an ultra-thin device layer that is highly doped. Due to the work function differences, the device layer volume depleted during the OFF state, thus, result in as extremely low leakage current. The gate modulates the resistance of the heavily doped semiconductor. Having said that, the word "transistor" actually came from the "trans-resistor", therefore, junctionless transistor works like a resistor controlled by the gate to allow the current flow [2].

Junctionless transistor lower than 10 nm gate length, an extraordinarily gradient of doping concentration is necessary. The fact that the junctionless transistor contain no junction, it helps the chipmakers to create smaller devices. It has less mobility degradation with temperature and gate voltage than the classical metal oxide semiconductor field effect transistor (MOSFET) [3]. No junction means a simpler fabrication process. The ON-state current for a 1µm channel length approximately the same as the conventional MOSFET, with insignificant drain induced barrier lowering (DIBL), and approximately ideal subthreshold slope [4]. This device said to be a suitable device for low power applications such as dynamic random access memory (DRAM) and static random access memory (SRAM) cells. Junctionless transistor exhibits lower ON-state current and prominent SCEs [5].

Silicon on Insulator (SOI) technology could further improve the ON-OFF state current ratio compared to the conventional technology. It has been concluded that junctionless transistor demonstrated low OFF-state current leading to high on-to-off state current ratio [6]. The combined the concept of SOI technology together with the single-gate junctionless transistor is referred as SOI-JLT. The combination of the two approaches, the on-to-off current ratio had been further improved as compared to the DGJLT [7].

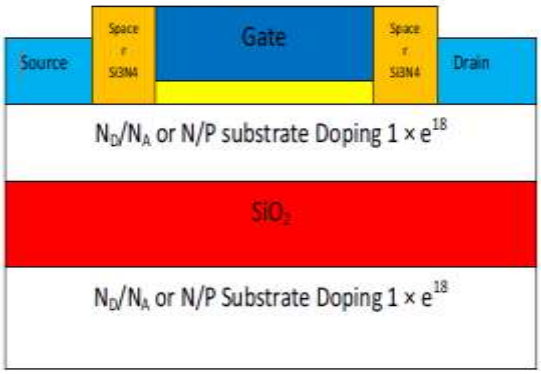

Fig. 2: Structure of SOI-JLT

The structure of the SOI-JLT shown in Fig. 2. The aim of this research is to analyse the performance of silicon-on-insulator based junctionless transistor for a conventional 6 transistor static random access memory (6T SRAM) cell at the same time minimizing the area consumption. The simulation of the research was done using the Sentaurus and Cogenda device simulator [8]. In this work, the electrical properties of the SOI-JLT was studied and used it to form the novel 6T SRAM cell and then extracted the performance of the novel 6T SRAM i.e. area

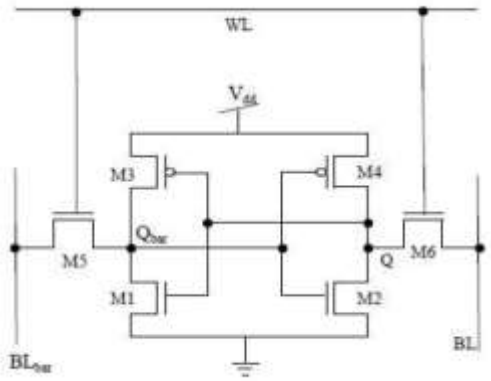

Fig. 3: 6T SRAM

Nanowire Junctionless Transistor (NJT) has gained overwhelming attention due to its structural advantages such as reduced short channel effect (SCE), low power consumption, and steep subthreshold swing. In this device, the most critical dimension that significantly affects the electrical properties of JLT are the gate length, oxide thickness as well as the critical thickness of strain even for one-dimensional (1D) device [9].

However, extreme scaling on these dimensions deteriorates the device's performance quality. Modern reduction of transistor has exponentially increased the density of SRAM in the system-on-chip (SoC). Hence, there is need to find different alternative for device structure in order to keep up with the increasing compactness of SRAM in SoC. Such compactness is a good thing since the SRAM utilize low supply voltage VDD, leading to ultra-low power consumption. Nevertheless, if the drain voltage, V_{DD} become too small, it will increase the SRAM delay performance and reduce its static noise margin (SNM) significantly. Moreover, SCEs becomes prominent in the nanoscale region due to unnecessary power consumption. Therefore, an SOI-NJT based 6T SRAM cell is proposed to improve the power dissipation and the delay in order to speed up the performance of the device, particularly in the read/write mode operation [10].

2.0. LITERATURE REVIEW

SCEs affect the performance of the MOSFET. Hence, revolution must be initiated in order to minimize the SCE. Therefore, new structure of the transistor such as the SOI technology, junctionless transistor, Gate-All-Around, Cylindrical MOSFET, Tri-gate FinFET, and many others were introduced by researchers. All of these structures have their own advantages and shortcomings [11].

This research will exclusively focus on the design of the 6T using the combination between the novel SOI-JLT. Therefore, the review will cover a little on junctionless transistor and SOI junctionless transistor and more on the performance comparison of SRAMs taken from different literatures [11].

There is no improvement in scaling in MuGJLT as compared to the MOSFET, as 5 – 20 nm was used in all the two simulations. DIBL and SS shows incredible improvement at a high gate length of 30 nm, but the aim of the scaling is to reduce the gate length not to increase. The electrical properties of JNT, inversion-mode transistor and accumulation-mode MOS devices for gate length 5nm were compared in 2011 by J.P. Colinge et al. The variation of threshold voltage with physical parameters and intrinsic device performed was analyzed [12]. Comparison between junctionless FET and core shell junctionless FET for a gate length of 7 – 20 nm and length from source to drain (Leff) of 25 nm has been conducted by Shubham Sahay and Mamidala Jagadesh Kumar. The electrical characteristics of Nanowire JLFET and core shell JLFET were compared [13].

The concept of SOI technology together with the single-gate junctionless transistor (referred as SOI-JLT). By combining these two approaches, the on-to-off current ratio had been further improved as compared to the DGJLT. The electrical properties of the SOI-JLT and used it to form the novel 6T SRAM cell. Then, the authors extracted the performance of the novel 6T SRAM i.e. area consumption and power consumption. The design of 6T SRAM using the SOI-JLT structure was proposed using a single-gate SOI-JLT supposed a highly reliable for SRAM application since it demonstrated a good behavior in term of on-to-off state current ratio, leading to low leakage power consumption. SOI-JLT in novel 6T SRAM successfully reduced the area consumption by nearly half of the conventional 6T SRAM [14].

Conventional 6T SRAM already denoted to exhibit the problem in read stability, where there was a chance of bit

flipping to occur during read mode. Such problem solved by using the 8T SRAM where the read and write mode were separated, thus increasing the overall SRAM stability. However, recently, Tripti Tripathi et al. had suggested a unique configuration of 8T SRAM to cope up with the problems in conventional 6T SRAM. The purpose of this literature was to improve the overall stability, speed, and leakage current performance of the conventional 6T SRAM. The simulations were done by using the Cadence Virtuoso on UMC 55 nm technology node. In the proposed novel conventional based 8T SRAM cell, the conventional 6T SRAM combined together with the multi-threshold CMOS (MTCMOS) and fingering techniques [15].

In the MTCMOS technique, two additional transistors with high threshold voltage (HVT) were added to the top and bottom of conventional 6T SRAM cell, to prevent the path from flow of current during the retention mode. The remaining six transistors were kept at low threshold voltage (LVT) to reduce the delay and power consumption at low voltage supply. On the other hand, the authors used fingering technique of transistor to reduce the diffusion area and perimeter [16].

3.0. RESEARCH METHODOLOGY

The research was initiated by identification of suitable physical parameter for SOI-JLT device. There are two sub-software used, which are Sentaurus Structure Editor (SDE), and Sentaurus Device (SDevice). The SDE is an interactive Graphical User Interface that foster the simpler environment to create the 2D and 3D transistor. It will be used to design the SOI-JLT p-MOS and n-MOS. As for the Sentaurus Device, the program mainly works on extracting the electrical performance of SOI-JLT. The program will act as device simulator to find each of the characteristics for each SOI-JLT n-MOS and p-MOS semiconductor design. The simulator can extract and analyze the SCEs parameters such as drain saturation current (Ion), leakage current (Ioff), DIBL, threshold voltage (Vth), and SS.

Simulations was performed for 180nm, 90nm, 65nm and 45nm technology nodes using SPICE simulator. The results obtained for the power dissipation and delay analyses carried out during read and write operations in SRAM using metal oxide semiconductor (MOS) and floating gate metal oxide semiconductor (FGMOS) are designed and simulated. To dealt with sub threshold operation we use drain voltage V_{dd} of 0.35V for all technology and techniques in this analysis. This reduces the power dissipation, making the SRAM cell applicable for low power applications, and the use of FGMOS further decreases the power dissipation and delay of the SRAM cell. Then, the gate-level schematic will then be placed under test bench and all the relevant simulation results are going to be analysed. In this phase, the simulation results only involve the functionality without the parasitic effects.

4.0. RESULT DISCUSSION

SRAM cell is a memory which has two stable states i.e. 0 and 1 in a logical circuit for data storage. The operation of the memory cell is quite simple because all the operations are performed by the single bit line. The cells are structured in the matrix form and each cell can be addressed individually. The data stored in the SRAM cells can read all the content at once with the help of column decoder. As the single bit line is connected to drain terminal of pass transistors, the tolerance capacity of noise margin gets improved. The bit lines will pass through 2 input nodes of access transistors, which control the cell stability during operations [8].

In this research, results for power dissipation were extracted for the two devices. MOS and FGMOS 6T SRAMs for 180nm, 90nm, 65nm and 45nm technology nodes for a constant Vdd of 0.35V. Fig. 4 shows the power dissipation for different node technologies. It was observed that 180nm technology node exhibits highest power consumption. However, as the gate length decreases further, power began to improved. 45nm technology demonstrated lowest power consumption. The result was also shown that power consumption decreases with lower technology node.

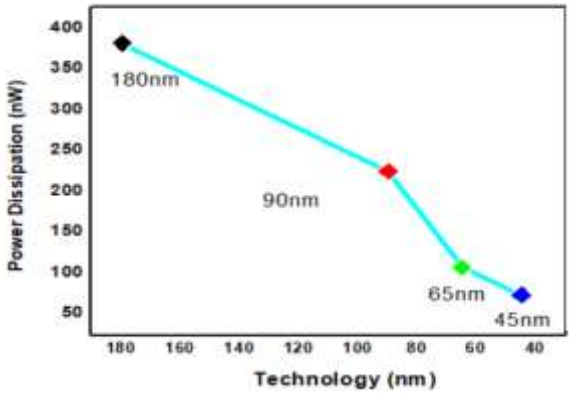

Fig. 4: Power Dissipation of a various Technology nodes for MOS device

In Fig. 5, the power dissipation of FGMOS device for different node technologies was shown 45nm technology have lowest power consumption. Nevertheless, high power consumption was revealed in 180nm technology. The lower the gate length, the lower the power consumption.

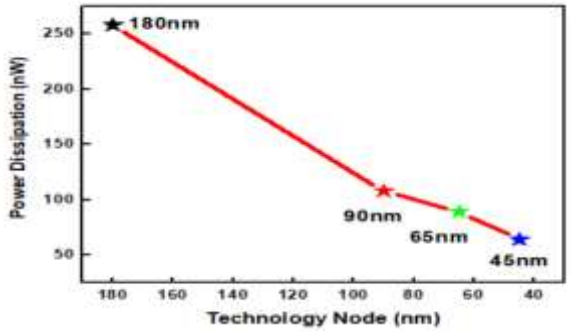

Fig. 5: Power Dissipation of a various Technology nodes for FGMOS device

The results obtained were compared and FGMOS 6T SRAM device demonstrated better power consumption a shown in fig 4 and 5 above. The power optimised and improved further when the lower technology nodes was used in the simulation. Fig. 6. Shows the read and write delay variation using MOS and FGMOS 6T SRAM devices for 180nm technology node. It was shown that techniques using FGMOS shows considerable decrease in read delay as compared to a device using MOS. Similarly, FGMOS device demonstrated considerable decrease in write delay as compared to device using MOS.

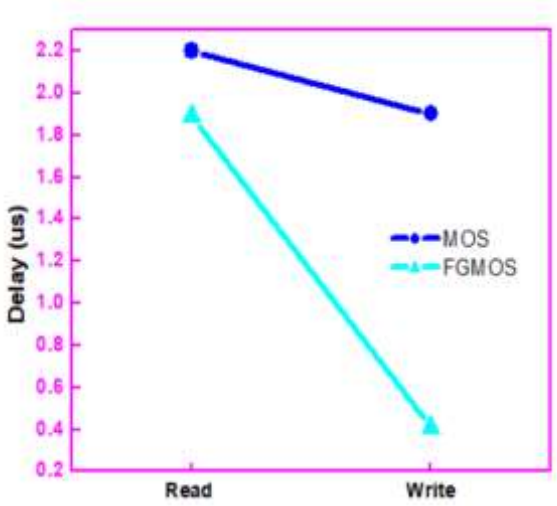

Fig. 6: Delay variations for MOS and FGMOS during Read/Write operations of 180nm Technology

5.0. CONCLUSION

In this Research, MOS and FGMOS based 6T SRAM of different technology nodes were designed and simulated at constant node voltage of 0.35V. Power dissipation was computed for different SRAM cell design techniques using MOS and FGMOS. Sub threshold operation is performed which helps to attain low power applications. It has been observed that 45nm technology node 6T SRAM cell demonstrated most optimized power dissipation as compared to 180nm, 90nm, and 65nm technology 6T-SRAM cells when we use MOS and FGMOS. In case of delay measurement, it was observed that device with FGMOS have most improved. Therefore, 6T SRAM device with FGMOS considerably decreases the power dissipation and delay of the SRAM cell more than MOS device, hence, improve the performance of the device.

6.0. ACKNOWLEDGMENT

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