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Design and Implementation of the Combinational Circuits Using Low Power Adiabatic Logic Techniques

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ABSTRACT: Power consumption in a circuit has been a major problem in the usage if devices and leads to serious issues of over battery or supply drain. On decreasing the circuit complexity the circuit needs to adapt to the real time world applications. In this paper, we propose a method so as to decrease power in the circuits that are used in real time, these methods are independent of the logic as they are in much reduced form, as compared to the normal static circuits.

KEYWORDS: Adiabatic, Pass Transistor Logic, Combinational Circuits, Power Consumption, Nmos Logic

I. INTRODUCTION

In present days, all the major electronic circuits and components involve the use of transistors both bipolar transistor and field effect transistors, the former ones being the most often used types in the electronic circuits. Their complexity is reduced till date as it helps majority of the users to have a portable device experience that can be used at any point of time. As the various devices used out in the world are movable, their circuitry is much reduced and is suitable to use in all kinds of situations. Several companies show interest in these areas of portable devices. As these devices are extensively used in real life these do not have to be of better performance as compared to the traditional circuits but have to be power efficient so as to save the battery which is of greater importance in these components. Some of the research in progress is regarding these designs of devices that are useful in real time and provide better power efficiency so as to be of much use in the real time use. So, the future of design of devices is based on these approximations and results in better loe power efficient device near provided it overcome challenges along with economic, social, legal acceptance.

We look forward to use the power reduction techniques so as to reduce the power consumption in a device and among all the available principles we use the adiabatic logic principle so as to reduce the power consumption across a circuit so as to reduce the power dissipation in a device. We intelligently reduce the power by replacing the irreversible conversion of the electric energy to heat that occurs due to the flow of current through the energy dissipative elements present in the circuit. This irreversible conversion is replaced by the conversion of the electrical energy to magnetic energy which can be achieved by use of AC supply at the power supply end.

II. RELATED WORK

We employed the logic circuits and designed a technique that reduces the power consumption across any circuit we desire to design. Several quasi adiabatic logic architectures have been reported such as ECRL, 2N-2N2P, PFAL, SCAL, and TSEL etc. Although they are suitable methods so as to reduce the power dissipated across the conventional CMOS circuits, but the charge of the output load that develops across the node capacitance is not completely discharged to ground.

These works are based on the concepts of "adiabatic NP-domino circuits' done by X.W.Wu, X.Lu and J.P.Hu. The "Low Power NMOS CPAL Circuits and Sequential Circuits" by Jianping Hu,Yinshui Xia ,Huiying Dong also is the another asset for this work done. "Pass-transistor adiabatic logic using single power clock supply" by V.G.Oklobdzija, D.Maksimovic and F.Lin ,and "True single phase adiabatic circuitry" by S.Kim, and M.C Papaefthymiou also are an asset for this work done.

III. METHODOLOGY

A. In any field effect transistor used we have the node capacitance that gets charged and discharged during its operation, for instance consider an inverter that is present and it has a node capacitance(C_L).For the transistors used, the current flow direction is based on the type of configuration used ,for instance the inverter used in the below figure (1) has a PMOS

that charges the node capacitance through the power supply Vdd ,and the NMOS .

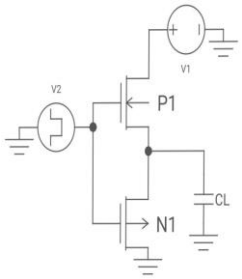


Figure-1 Normal CMOS Inverter

Transistor discharges the charged capacitance to ground .The discharge and charging of the node capacitance CL leads to the power loss across the transistor which is avoided by using the below methods.

B. CPAL

The CPAL technique employs a basic unit of design for all the gates that are to be used and implemented, it consists of PMOS and NMOS Transistor. The structure consists of 2 blocks

1. The logic block
2. The load driving circuit block

The logic block consists of a total 4 NMOS transistors that employ complementary pass Transistor Logic and decide the logic to be implemented in the base unit. For instance consider the inverter shown below figure (2)

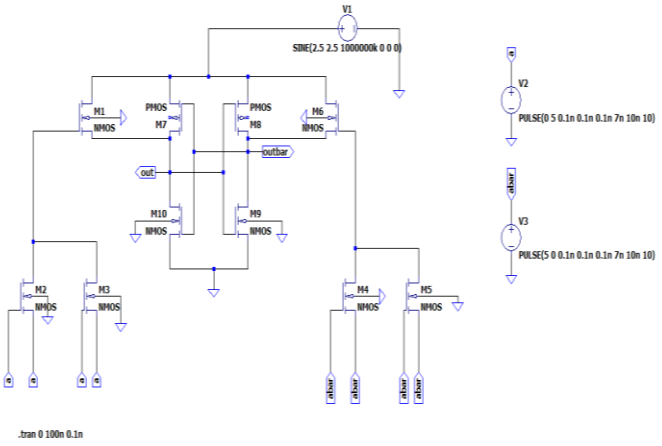


Figure-2(a) CPAL Inverter

The load driving part consists of the output that are connected back to back, where we get the output and a complement version of the same resultant output. There are 2 clamped Transistors that are used to clamp the unground output at output nodes to zero.

The MN4 and MN3 NMOS Transistors are acting as clamped circuits. The buffer output is seen at OUT and the inverter output is seen at the OUT``.

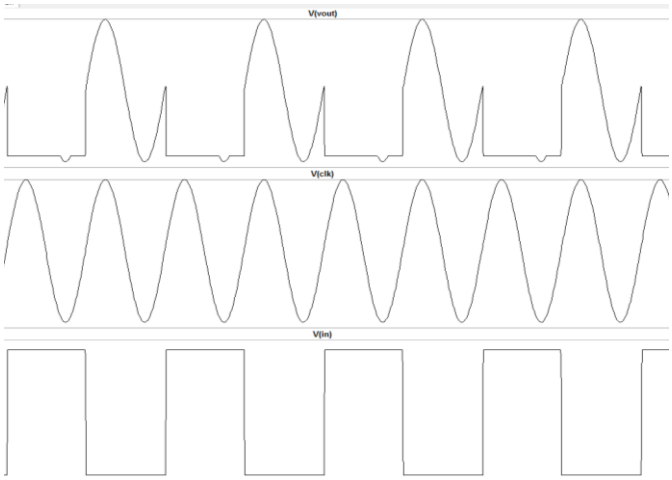


Figure-2(b) CPAL inverter waveforms

C. PFAL

The PFAL approach employs the design similar to that of CPAL but in this case two inverters are connected back to back. The structure consists of sane 2 blocks

1. The logic block
2. The load driving circuit block

The logic block consists of a total 4 NMOS transistors that employ positive feedback adiabatic logic and decide the logic to be implemented in the base unit. For instance consider the inverter shown below figure (3)

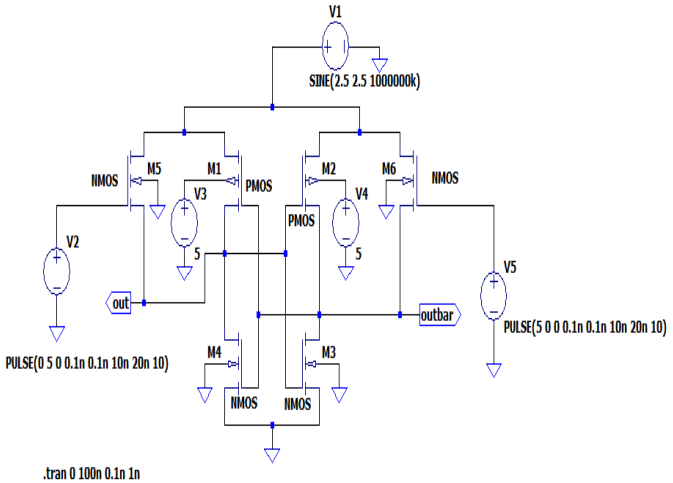


Figure-3(a) PFAL Inverter Wave forms

The load driving part consists of the output that are connected back to back, where we get the output and a complement version of the same resultant output. There are 2 clamped Transistors that are used to clamp the unground output at output

nodes to zero. Here there is no PMOS present at the load driving side as it gets turned on only during clock cycle is 1, it is omitted and the result structure resembles the Bootstrapped NMOS design.

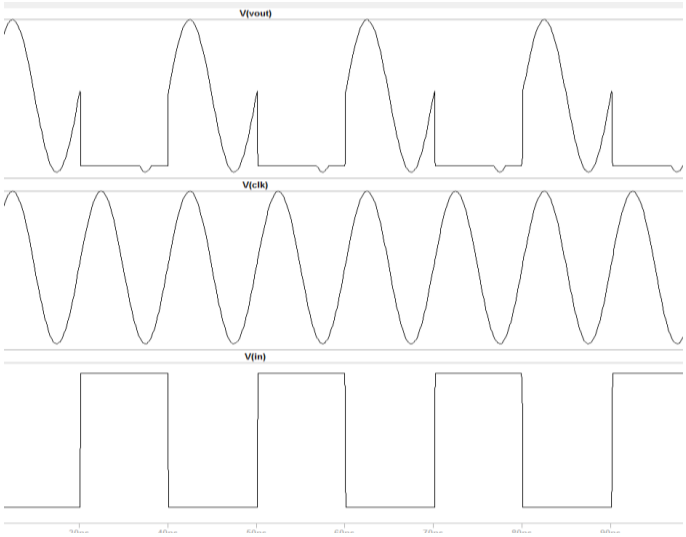


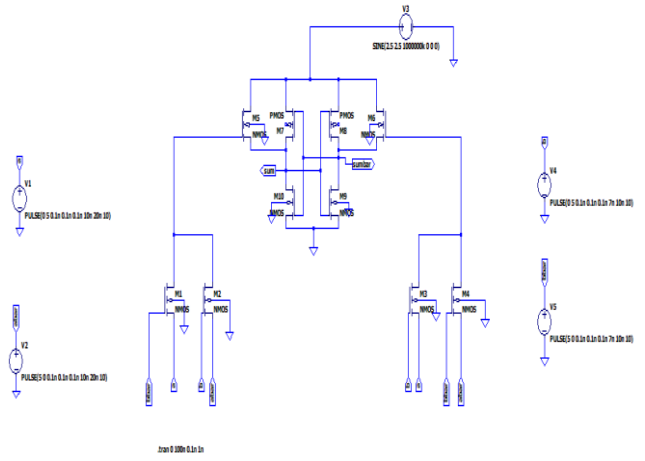
Figure-3(b) PFAL Inverter Wave forms

D. COMBINATIONAL CIRCUITS

All the combinational circuits are implemented by changing only the logic part in the CPAL and PFAL Techniques so the circuitry doesn't change but the output changes with respect to changes provided in the input.

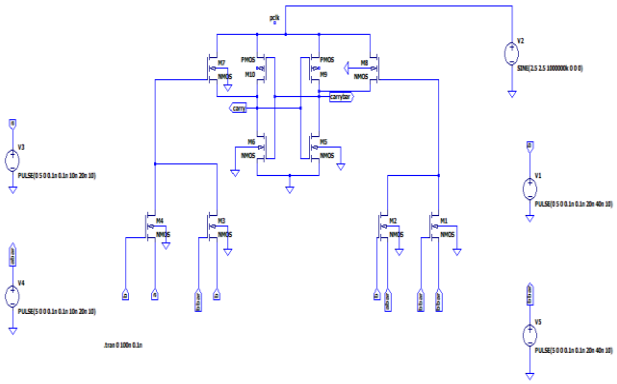
All the combinational circuits are shown below using CPAL

1. HALF ADDER SUM



4(a)- In half adder two inputs are given and the sum of it is given as output. Binary addition is performed. Output equation for Sum = A XOR B

2. HALF ADDER CARRY

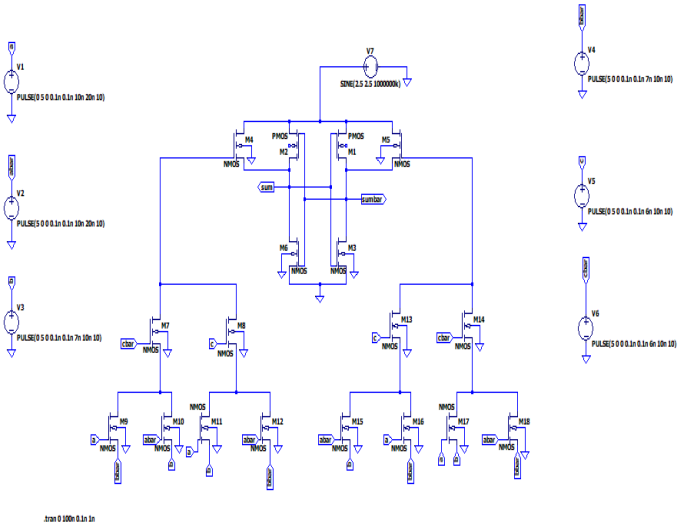


4(b)- In half adder two inputs are given and the carry of it is given as output.Expression for half adder Carry = A **AND B**

Inputs		Outputs	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

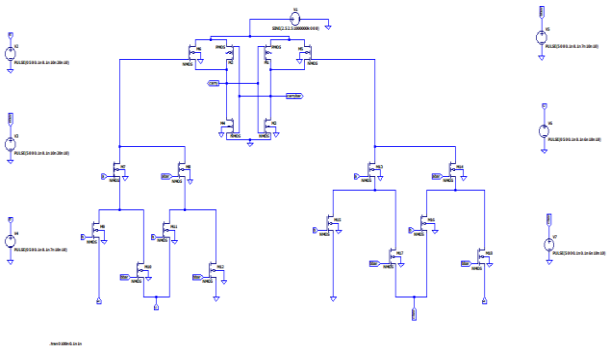
Table 4(a)-Truth table of half adder representing sum and carry.

3. FULL ADDER SUM



4(c)- In full adder three inputs are given and the sum of it is given as output. Binary addition is performed.Expression for Sum= A ⊕ B ⊕ Cin

4. FULL ADDER CARRY

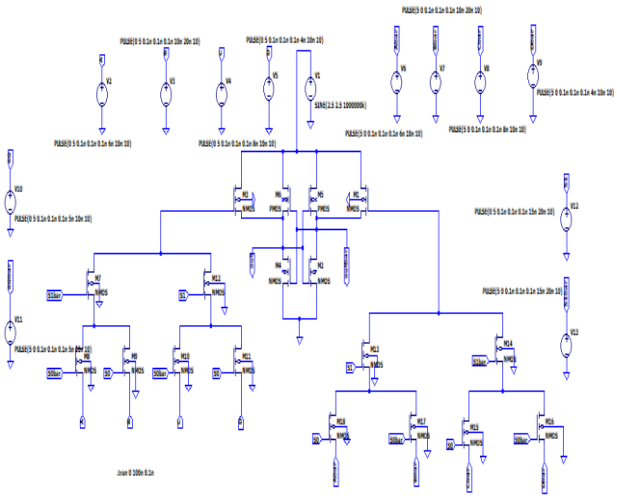


4(d)- In full adder three inputs are given and the carry of it is given as output. Expression is given as Carry=AB + Cin (A ⊕ B)

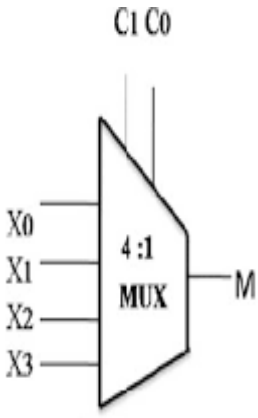
Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 4(b)-Truth table of full adder showing sum and carry.

5. 4X1 MULTIPLEXER



4(e)- The multiplexer is a combinational logic circuit designed to switch one of several input lines to a single common output line. Output equation is given as Y = S1′S0′I0 + S1′S0I1 + S1S0′I2 + S1S0I3

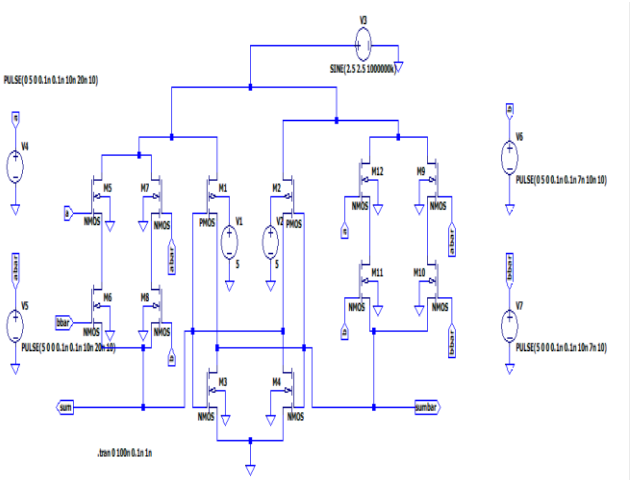


C1	C0	M
0	0	X0
0	1	X1
1	0	X2
1	1	X3

Table 4(c)-4x1 Multiplexer truth table.

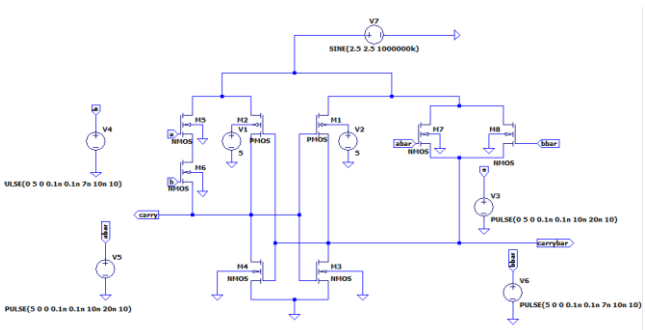
All the combinational circuits are shown below using PFAL.

1. HALF ADDER SUM



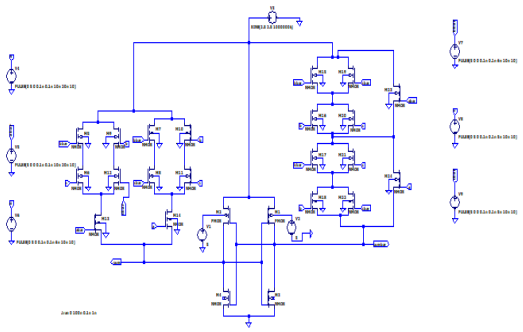
4(f)-Half adder sum designed using PFAL

2. HALF ADDER CARRY



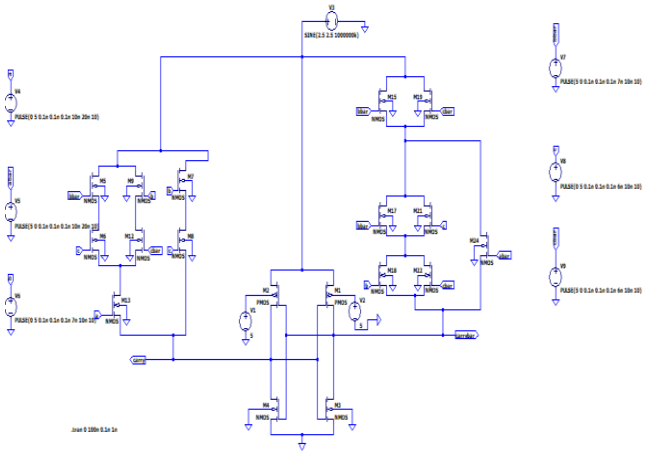
4(g)- Half adder carry designed using PFAL

3. FULL ADDER SUM



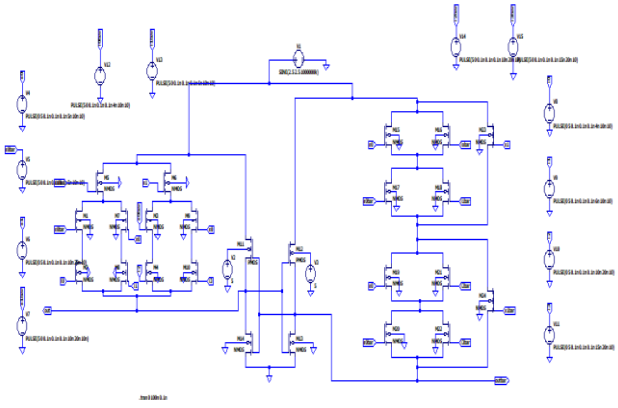
4(h)-Full adder sum is implemented in PFAL logic

4. FULL ADDER CARRY



4(i)- Full adder carry is implemented in PFAL logic

5. 4X1 MULTIPLEXER



4(j)- 4x1 Multiplexer is implemented using PFAL logic

IV. UNITS

As we deal with the power consumption across a transistor the preferred units in the SI unit system are Watts(W).These magnitudes are in ranges of Nano(nW) and Micro watts(mW) and some times leads to the Pico Watts (pW).

V.RESULTS ANALYSIS

TYPE OF ADIABATIC LOGIC USED	CPAL		PFAL	
CIRCUIT	PMOS	NMOS	PMOS	NMOS
HALF ADDER SUM	70µw	200 µw	12 µw	80 µw
HALF ADDER CARRY	60 µw	140 µw	50pw	80 µw
FULL ADDER SUM	100 µw	200 µw	30 µw	60 µw
FULL ADDER CARRY	90 µw	170 µw	12 µw	80 µw
4 X 1 MULTIPLEXER	300 µw	400 µw	140 µw	200 µw

Table 5(a)-Table representing the comparison results of combinational circuits using CPAL and PFAL technique.

We preferably reduce the power dissipated across the transistors used across the combinational logic circuits implemented.

VI. CONCLUSION

We have successfully implemented the combinational using the above 2 logic techniques and this helps us to identify the suitable methods used to reduce power consumption across the transistors used and there by increases the efficiency of the circuit.

POWER DISSIPATED ACROSS CPAL LOGIC DESIGN

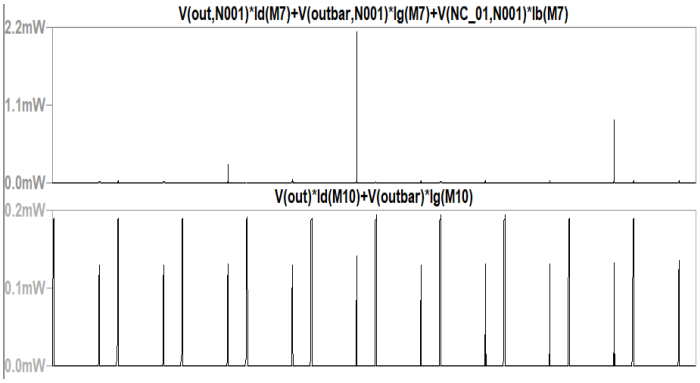


Figure (6)-a. power dissipated in CPAL circuit vs. the time period of operation

POWER DISSIPATED ACROSS PFAL LOGIC DESIGN

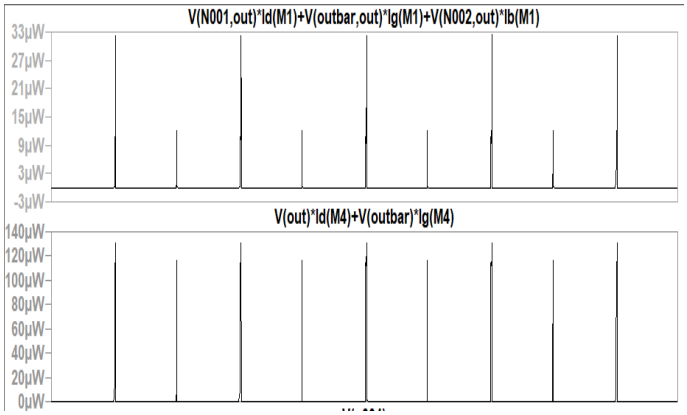


Figure (6)-b. power dissipated in PFAL circuit vs. the time period of operation

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